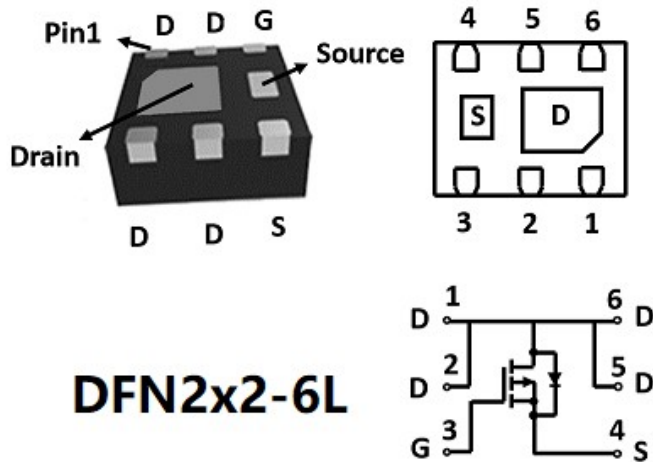


## P-Channel Enhancement Mode Field Effect Transistor



### Product Summary

- $V_{DS}$  -20V
- $I_D$  -16A
- $R_{DS(ON)}$ ( at  $V_{GS} = -4.5V$ ) <19mohm
- $R_{DS(ON)}$ ( at  $V_{GS} = -2.5V$ ) <22mohm
- $R_{DS(ON)}$ ( at  $V_{GS} = -1.8V$ ) <30mohm

### General Description

- Trench Power MV MOSFET technology
- High density cell design for Low  $R_{DS(ON)}$
- High Speed switching

### Applications

- Battery protection
- Load switch
- Power management

### ■ Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Maximum	Unit
Drain-source Voltage	$V_{DS}$	-20	V
Gate-source Voltage	$V_{GS}$	$\pm 10$	V
Drain Current	$I_D$	$T_C=25^\circ C$ @ Steady State	-16
		$T_C=70^\circ C$ @ Steady State	-12.8
Pulsed Drain Current <sup>A</sup>	$I_{DM}$	-64	A
Total Power Dissipation @ $T_C=25^\circ C$	$P_D$	18	W
Thermal Resistance Junction-to-Case @ Steady State	$R_{\theta JC}$	6.9	$^\circ C/W$
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~+150	$^\circ C$

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ1216A	F1	Q1216	3000	30000	120000	7" reel



# YJQ1216A

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA	-20			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V, T <sub>C</sub> =25°C			-1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±10V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =-250μA	-0.4	-0.62	-1.0	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = -4.5V, I <sub>D</sub> =-10A		11	19	mΩ
		V <sub>GS</sub> = -2.5V, I <sub>D</sub> =-6.5A		14	22	
		V <sub>GS</sub> = -1.8V, I <sub>D</sub> =-4.0A		20	30	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =-13A, V <sub>GS</sub> =0V		-0.8	-1.2	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				-13	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-10V, V <sub>GS</sub> =0V, f=1MHZ		2992		pF
Output Capacitance	C <sub>oss</sub>			330		
Reverse Transfer Capacitance	C <sub>rss</sub>			272		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-15V, I <sub>D</sub> =-9.1A		72.8		nC
Gate Source Charge	Q <sub>gs</sub>			6.6		
Gate Drain Charge	Q <sub>gd</sub>			10.1		
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =-6A, di/dt=100A/us		34		
Reverse Recovery Time	t <sub>rr</sub>			67		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-15V, I <sub>D</sub> =-6A, R <sub>GEN</sub> =2.5Ω		7		ns
Turn-on Rise Time	t <sub>r</sub>			33		
Turn-off Delay Time	t <sub>D(off)</sub>			130		
Turn-off Fall Time	t <sub>f</sub>			132		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design, while R<sub>θJA</sub> is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



■ Typical Performance Characteristics

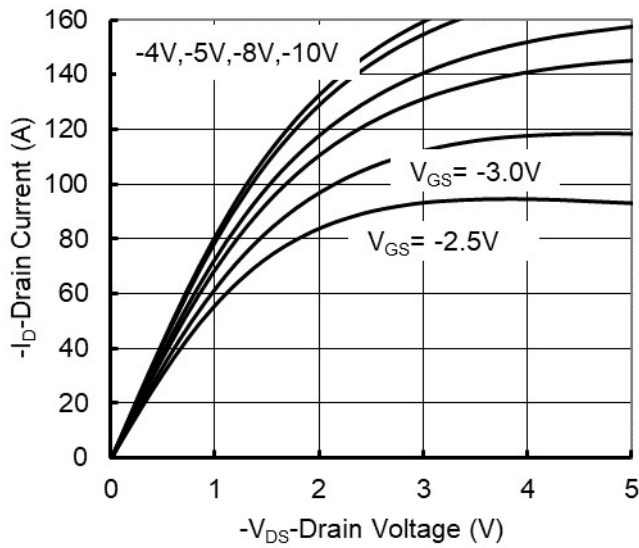


Figure 1. Output Characteristics

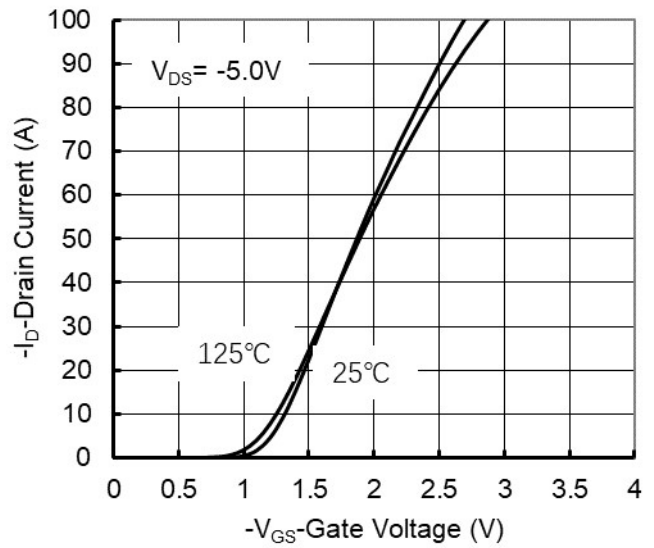


Figure 2. Transfer Characteristics

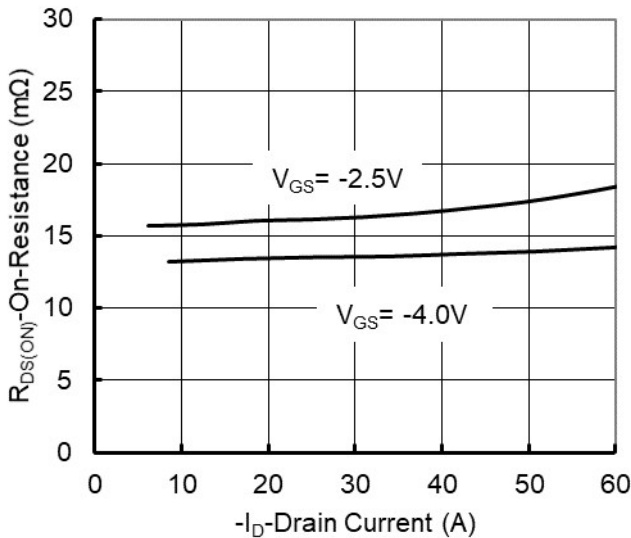


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

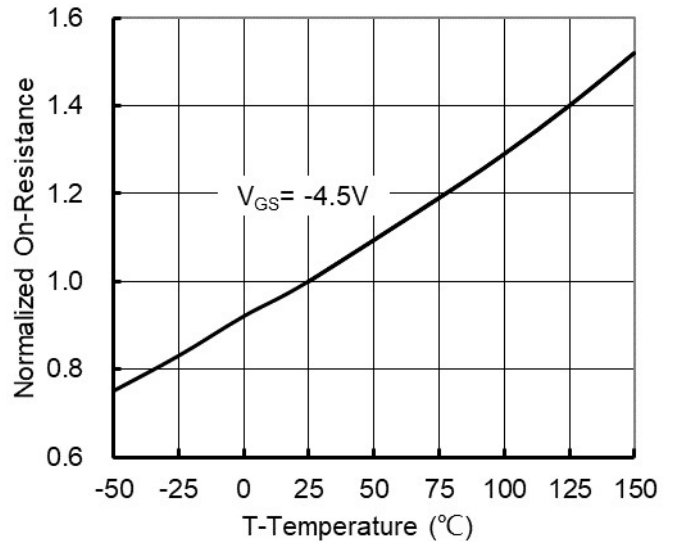


Figure 4. On-Resistance vs. Junction Temperature

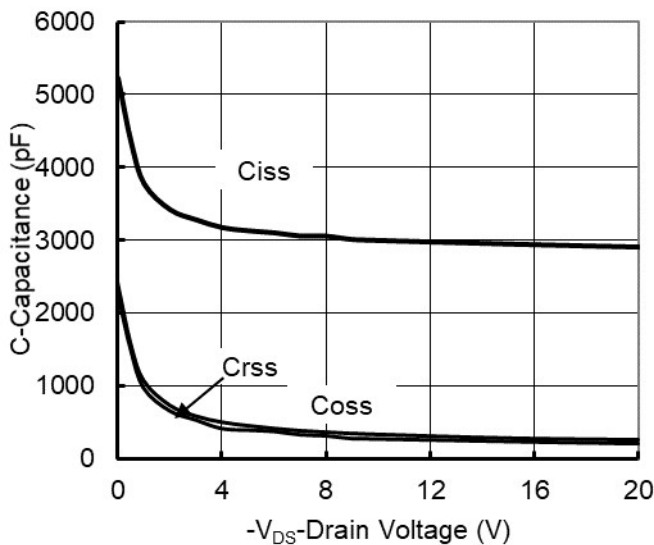


Figure 5. Capacitance Characteristics

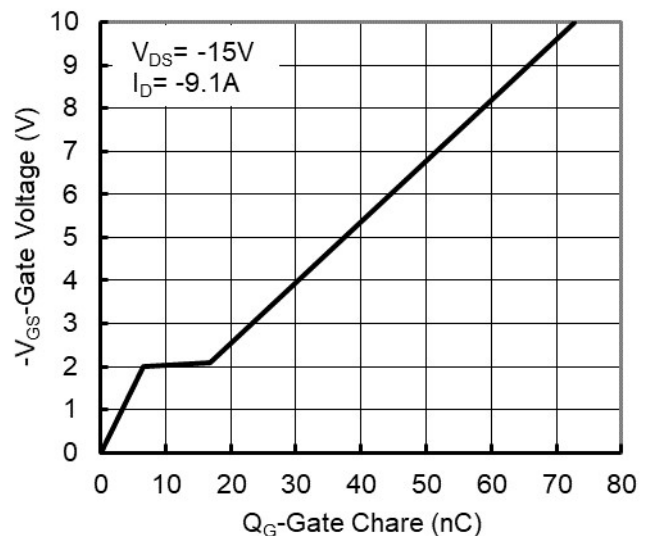


Figure 6. Gate Charge

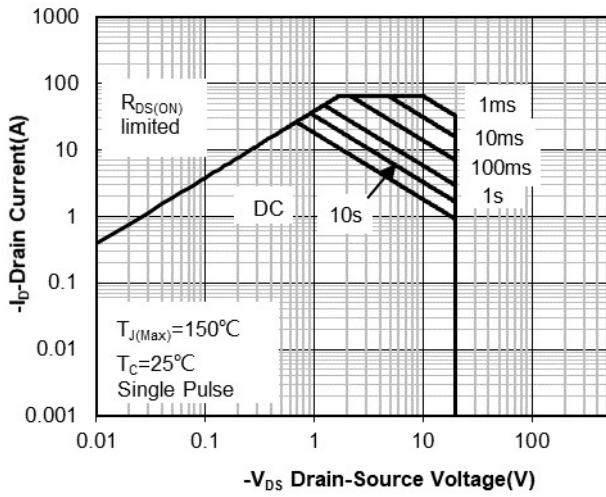


Figure 7. Safe Operation Area

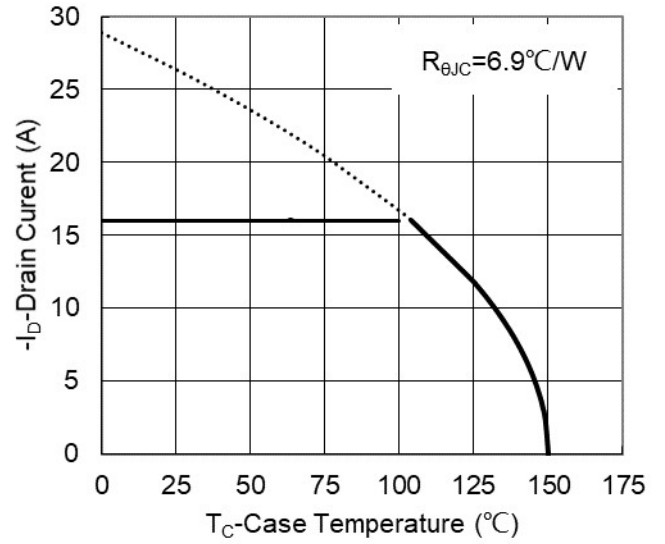
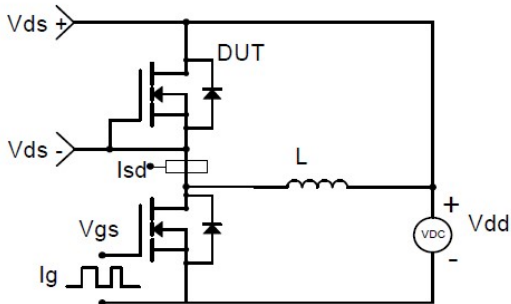


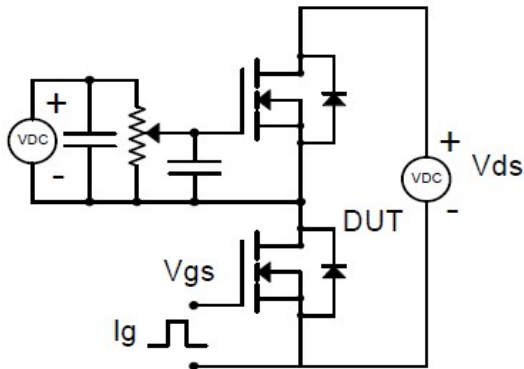
Figure 8. Maximum Continuous Drain Current vs Case Temperature



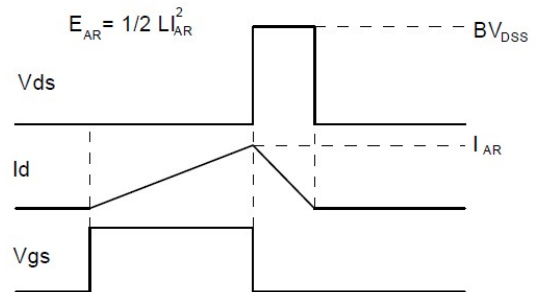
**Resistive Switching Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



**Gate Charge Test Circuit & Waveform**

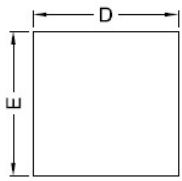


**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**

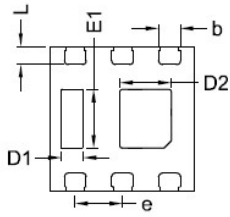


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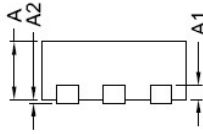
## ■DFN2x2-6L(0.80mm) Package information



Top View  
正面视图

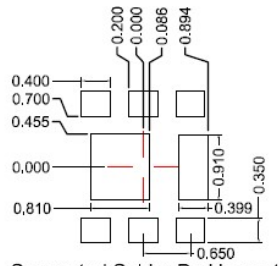


Bottom View  
背面视图



Side View  
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	1.90	2.00	2.10
E	1.90	2.00	2.10
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	0.20	0.30	0.40
D2	0.61	0.71	0.81
E1	0.71	0.81	0.91
L	0.15	0.25	0.35
b	0.20	0.30	0.40
e	0.65 BSC		



Suggested Solder Pad Layout  
Top View

Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.10$ mm.
3. The pad layout is for reference purposes only.



# YJQ1216A

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