Over–Voltage Protection IC

Description

The JXW1605B Over-Voltage Protection device features a very low R_{DS_ON} resistance, typical 48mΩ, internal nFET for USB VBUS line. The nFET switch ensures safe and right current flow in both charging and host modes such as OTG while protecting the internal system circuits from any over voltage conditions. Over-voltage threshold can be adjusted externally with a resistor divided network, or set internally by the built-in value.

The device features an open-drain output nACK, when $V_{IN\_UVLO} < V_{IN} < V_{IN\_OVLO}$ and the switch is on, nACK will be driven low to indicate a good power input, otherwise it is high impedance.

This device features over-temperature protection that prevents itself from thermal damaging. The device operates over a -40°C to +85°C ambient temperature range.

The JXW1605B is available in a RoHS and Green compliant DFN2x2-6L package.

Features

- A Very Low R_{DS_ON} 48mΩ (typ.) n-Channel MOSFET
- Adjustable OVP Threshold from 4V to 20V
- Default Threshold Voltage
  - ◊ 6.0V for JXW1605B
- VBUS DC Input Voltage Range : 2.8V ~ 32V
- 4A Max Continuous Current Capability
- OTG Functionality on VBUS Path
- Active-low Switch Status Indicator Output
- Pass IEC61000-4-2 ESD for V_{IN} Port
  - Contac discharge: ±8KV
  - Air discharge: ±15KV
- DFN2x2-6L package

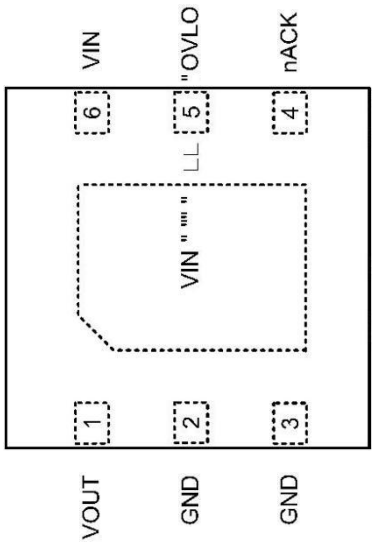
Applications

- Mobile Handsets
- Tablets
- Wearable Devices
- Charging Ports

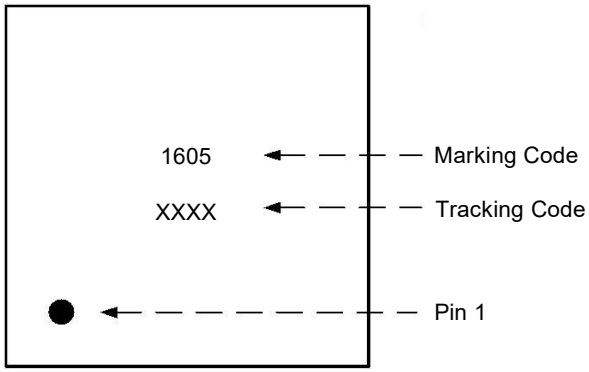
Device Comparison Table and Ordering Information

Model	Order Number	Package	Operation Ambient Temperature	Shipping Option	Marking	V_{IN_OVLO}
JXW1605B	JXW1605BDFT	DFN-2x2-6L	-40°C ~ 85°C	3000/Tape & Reel	1605XXXT	6.0V

Pin Configuration and Top Mark



Top View

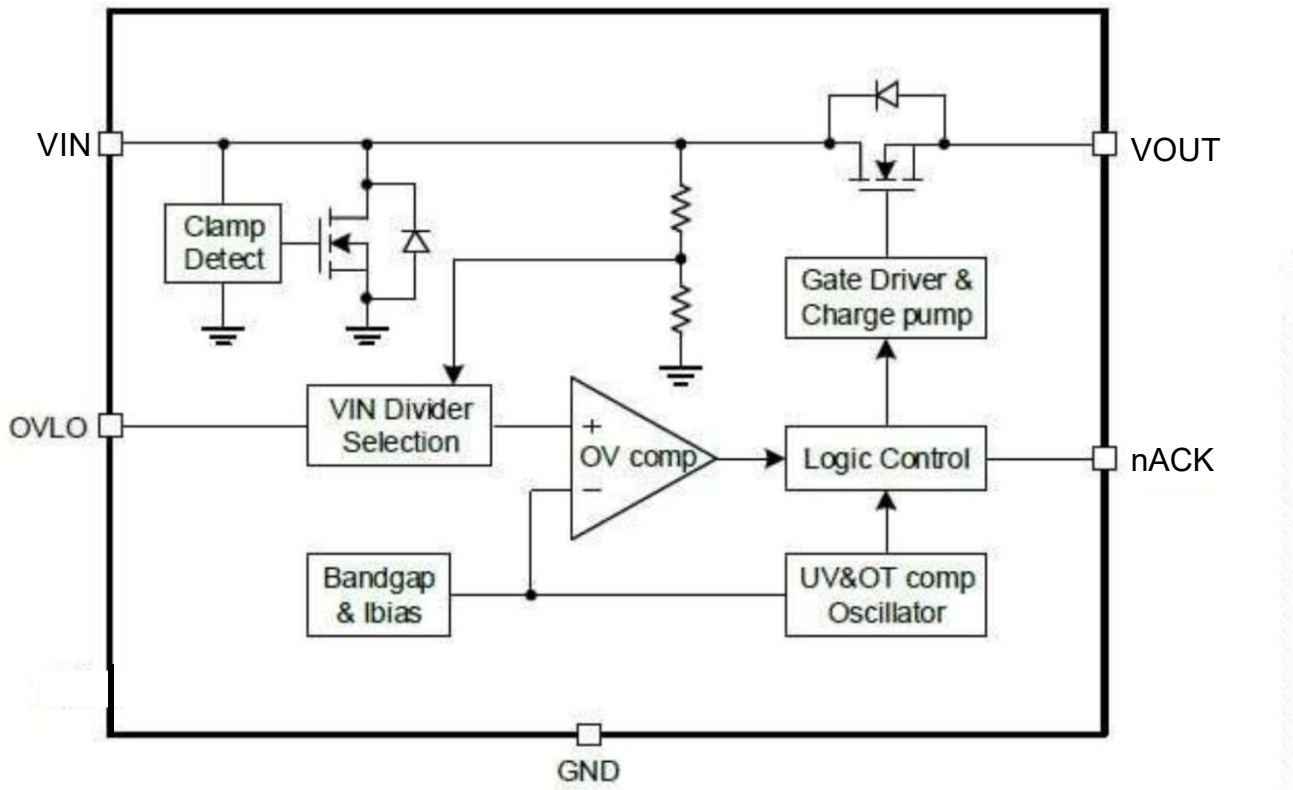


Top Mark

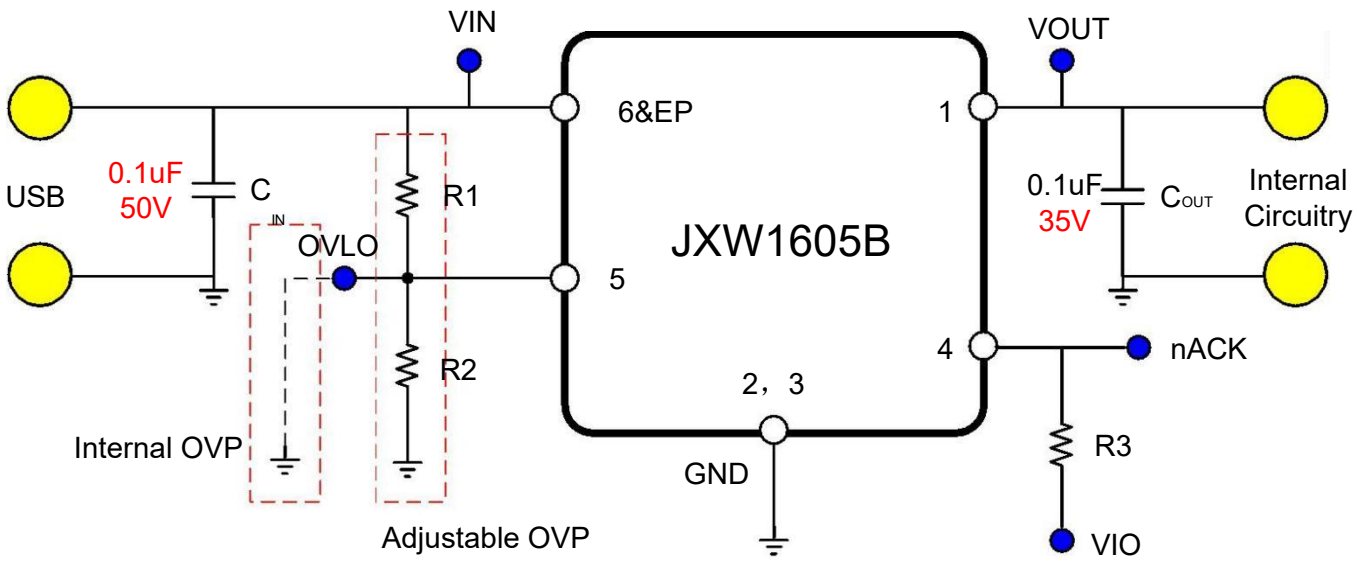
Pin Assignments

Pin	Name	Description
1	V_{OUT}	Output Voltage：bypass with a 0.1uF/35V ceramic capacitor as close to the device as possible. Capacitor breakdown voltage selected is depended on OVLO threshold set.
2	GND	Ground
3	GND	Ground
4	nACK	Open-Drain Active-Low Output ： Active-low logic output. It needs an external pull-up resistor, e.g.10kΩ ~ 470 kΩ, to the System I/O. If not used，leave it open or tied to ground.
5	OVLO	OVP Threshold Adjustment ： Connect the pin to ground to use a fixed internal threshold. Connect a resistor-divider to set a different threshold between 4V and 20V.
6	V_{IN}	Voltage Input：bypass with a 0.1uF/50V ceramic capacitor as close to the device as possible.
EP	V_{IN}	Voltage Input：Need to short to Pin 6 with wide metal trace.

Functional Block Diagram



Typical Application Circuit



Absolute Maximum Ratings (T_A= 25°C unless otherwise specified)

Parameter	Symbol	Min	Max	Unit
Input DC voltage	V_{IN}	-0.3	36	V
Output voltage	V_{OUT}	-0.3	24	V
OVLO voltage	V_{OVLO}	-0.3	7	V
nACK voltage	V_{ACK}	-0.3	7	V
Switch current (Continuous current)	I_{IN}		4	A
Ambient temperature	T_A	-40	85	°C
Junction temperature	T_J	-40	125	°C
Storage temperature	T_{STG}	-55	150	°C
Soldering temperature (At leads，10 seconds)	T_{LEAD}		260	°C

Thermal Information

Parameter	Symbol	Value	Unit
Thermal resistance from junction to ambient (In free air)	$R_{\Theta JA}$	70	°C/W

Operating Conditions

Parameter	Symbol	Min	Max	Unit
Input DC Voltage	V_{IN}	2.8	32	V
Input Capacitance	C_{IN}	0.1		uF
Output Load Capacitance	C_{OUT}	0.1	100	uF
Human Body Model	V_{ESD}	-2	2	kV
Charged Device Model		-500	500	V
Machine Model		-200	200	V
Latch-up	$I_{Latch-up}$	-200	200	mA
Contact discharge for IEC61000-4-2 standard	V_{IN_PORT}	-8	+8	KV
Air discharge for IEC61000-4-2 standard	V_{IN_PORT}	-15	+15	KV

Electrical Characteristics (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Switch on resistance	R_{DS_ON}	V_{IN} = 5V, I_{OUT} = 1A		48	58	mΩ
		V_{IN} = 3.3V, I_{OUT} = 1A		53	63	mΩ
Input quiescent current	I_Q	V_{IN} = 5V, V_{OVLO} = 0V, I_{OUT} = 0A		105	130	uA
Input current at over-voltage condition	I_{IN_OVLO}	V_{IN} = 5V, V_{OVLO} = 3V, V_{OUT} = 0V		93	130	uA
OVLO set threshold	V_{OVLO_TH}		1.16	1.20	1.24	V
OVP threshold adjustable range	V_{OVLO_RNG}		4		20	V
External OVLO select threshold	V_{OVLO_SEL}	OVLO Rising	0.26	0.29	0.32	V
		Hysteresis		0.04		
OVLO pin leakage current	I_{OVLO}	V_{OVLO} = V_{OVLO_TH}	-0.1		0.1	uA

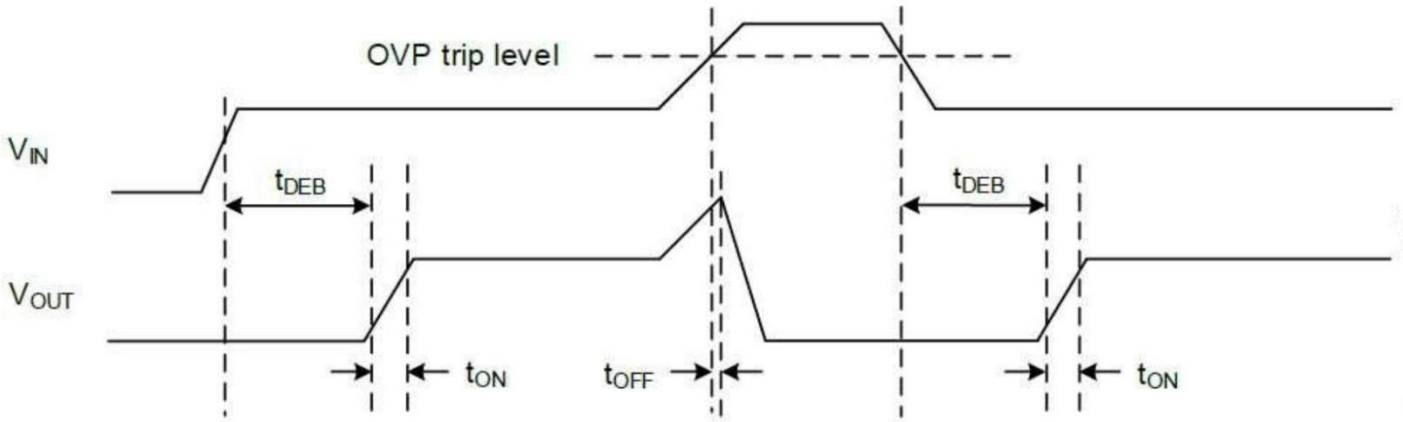
Electrical Characteristics (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Protection							
OVP trip level	V_{IN_OVLO}	JXW1605B	V_{IN} rising	5.88	6.0	6.12	V
			Hysteresis		0.15		
UVLO trip level	V_{IN_UVLO}	V_{IN} rising				2.8	V
		V_{IN} falling		2.2			
Shutdown temperature	T_{SDN}				140		°C
Shutdown temperature Hysteresis	T_{SDN_HYS}				30		°C

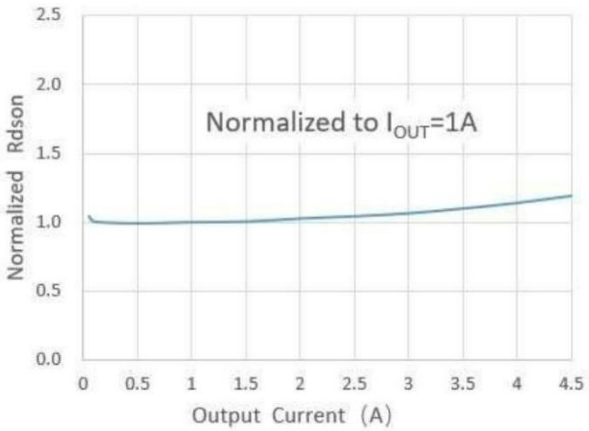
Electrical Characteristics (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Timing Characteristics						
Debounce time	t_{DEB}	From V_{IN} > V_{IN_UVLO} to 10% V_{OUT}		23		ms
Switch turn-on time	t_{ON}	R_{OUT} = 100Ω, C_{OUT} = 0.1μF, V_{OUT} from 10% V_{IN} to 90% V_{IN}		0.8		ms
Switch turn-off time	t_{OFF}	R_{OUT} = 100 Ω,C_{OUT} = 0.1μF,V_{IN} > V_{IN_UVLO} to V_{OUT} stop rising, V_{IN} rise at 10V/μs		90		ns

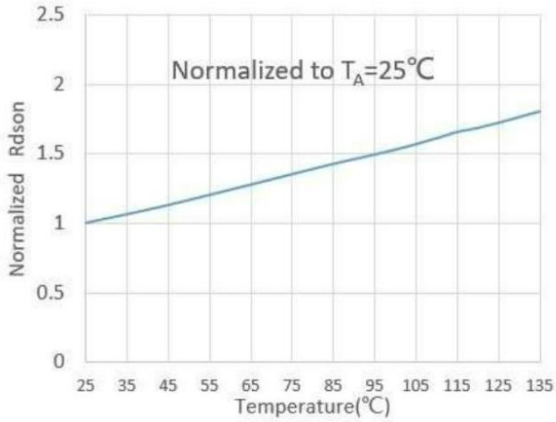
Timing Diagram



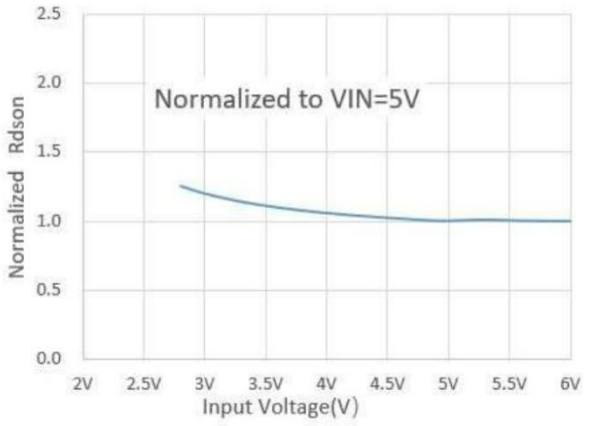
Typical Performance Characteristics (V_{IN} = 5V, C_{IN} = C_{OUT} = 0.1uF, T_A = 25°C)



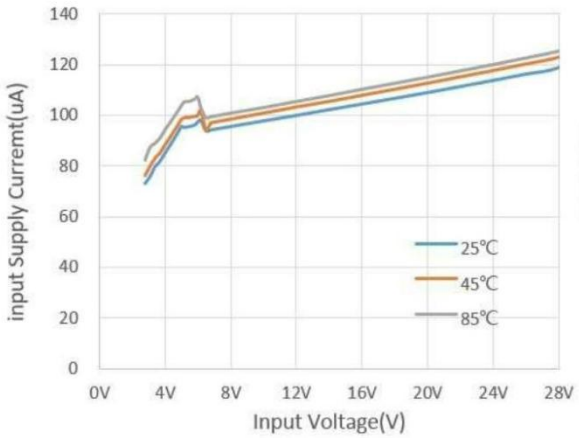
Normalized R_{DS_ON} vs Output Current. (VIN=5V)



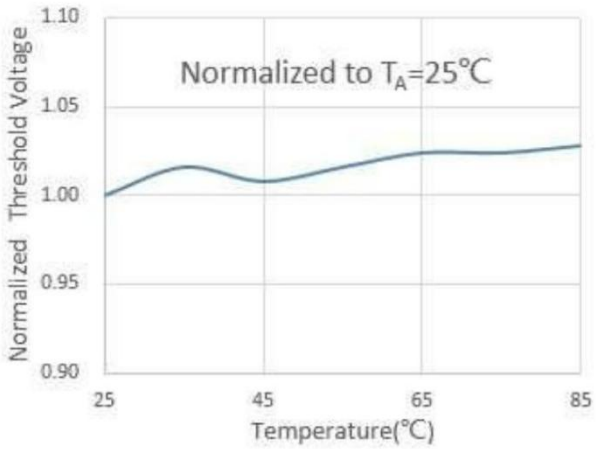
Normalized R_{DS_ON} vs Temp. (I_{OUT}=1A)



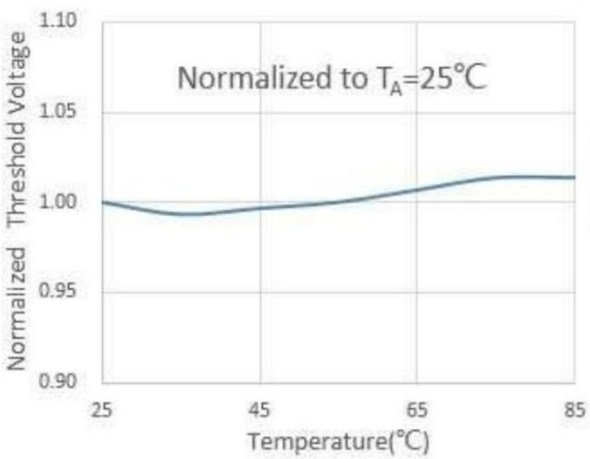
Normalized R_{DS_ON} vs Input Voltage (I_{OUT}=1A)



Input Supply Current vs Supply Voltage

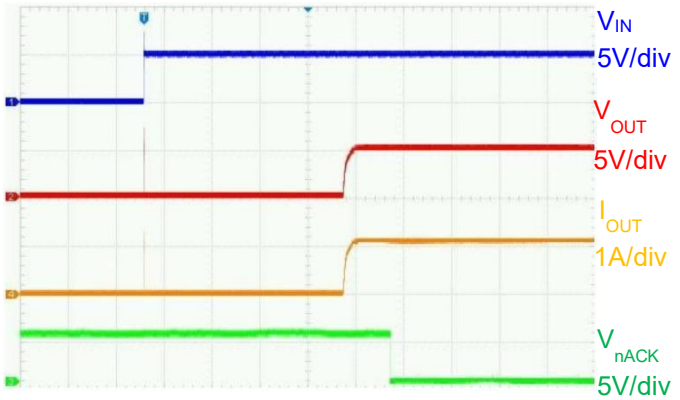


Normalized Internal OVP Threshold

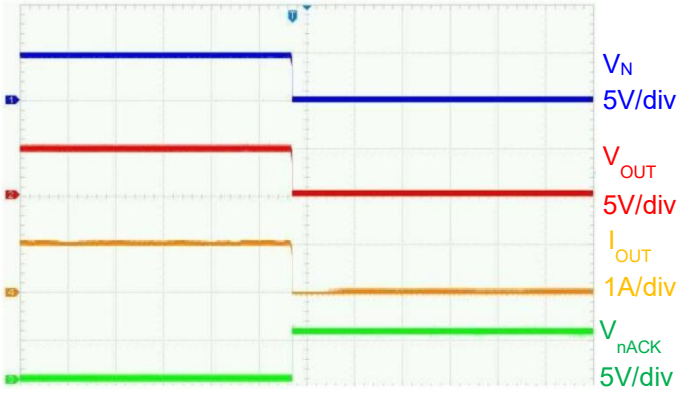


Normalized External OVP Threshold

Typical Performance Characteristics (V_{IN} = 5V, C_{IN} = C_{OUT} = 0.1uF, R_{OUT} = 100Ω， T_A = 25°C）

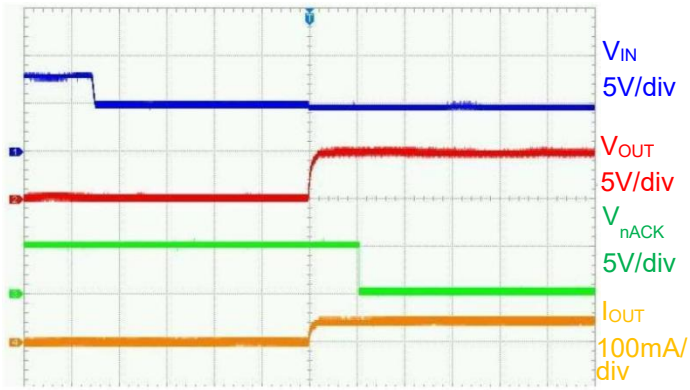


Power-up (1A load)



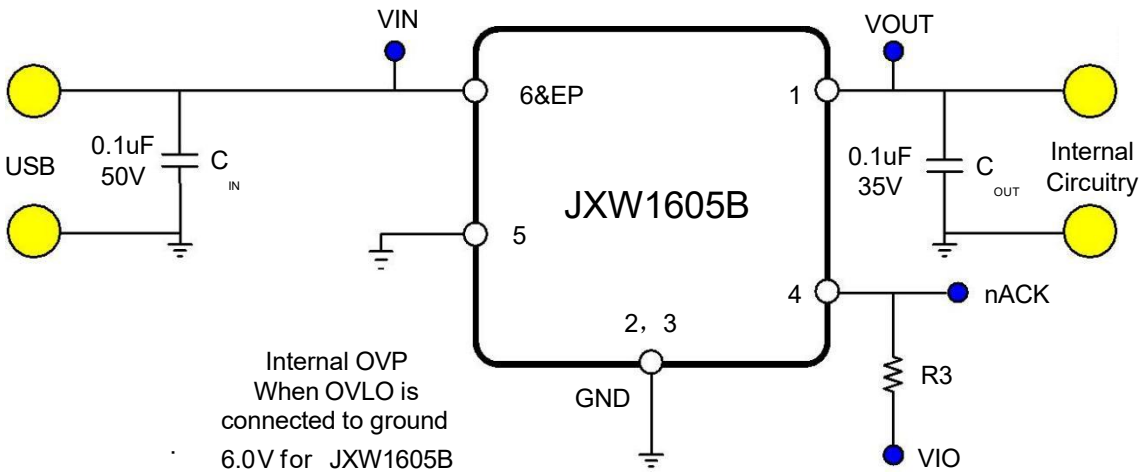
Power-down (1A load)

OVP Response

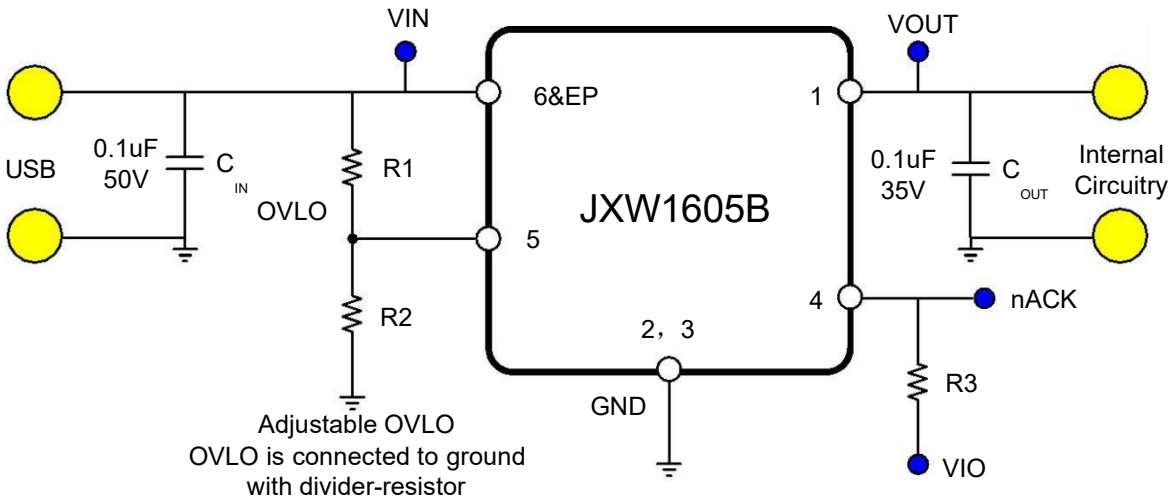


Recovery from OVP

Typical Application circuit



Fixed OVP circuit



VIN_OVLO = (R1+R2)/R2*VOVLO_TH，where VOVLO_TH value is 1.20V(TYP.)
OVLO Pin voltage is more than 0.29V(TYP.)

Adjustable OVP circuit

Functional Description

Device Operation

If the input voltage is between UVLO and OVP threshold, the internal charge pump begins to work after debounce time, the gate of the nFET switch will be slowly charged high till the switch is fully on. If the input voltage exceeds the OVP trip level, the switch will be turned off in about 90ns. If input voltage falls below UVLO threshold, or over-temperature happens, the switch will also be turned off.

Over-Voltage Protection

If the input voltage exceeds the OVP rising trip level, the switch will be turned off in about 90ns. The switch will remain off until V_{IN} falls below the OVP falling trip level.

OVP Threshold Adjustment

If OVLO pin is not grounded, and by connecting external resistor divider to OVLO pin as shown in the typical application circuit, between IN and GND, the OVP threshold can be set as following formula:

$$V_{IN\_OVLO} = (R_1+R_2) / R_2 * V_{OVLO\_TH}$$

The adjustment range is 4V to 20V. When the OVLO pin voltage V_{OVLO} exceeds V_{OVLO_SEL} (0.29V typical), V_{OVLO} is compared with the reference voltage V_{OVLO_TH} (1.2V typical) to judge whether input supply is over-voltage.

USB On-The-Go (OTG) Operation

If V_{IN} = 0V and OUT is supplied by OTG voltage, the body diode of the load switch conducts current from OUT to IN and the voltage drop from OUT to IN is approximately 0.7V. When $V_{IN} > V_{IN\_UVLO}$, internal charge pump begins to open the load switch after debounce time. After switch is fully on, current is supplied through switch channel and the voltage drop from OUT to IN is minimum.

Load Switch Status Indicator

The device has a load switch status indicator to notify load switch on/off status to other devices. When load switch is on status, the device pulls nACK pin down to the GND.

Thermal Protection

The device has an Over-Temperature Protection circuit to protect device against system fault or improper use. When the junction temperature exceeds the threshold, 140°C typical, the device shuts down and stays off until the temperature cools down to a safe region (below falling threshold). Once the falling threshold, the device will automatically resume the normal operation with embedded timings.

Device Operation Summary

Conditions		Operations			
V_{IN}	V_{OUT}	Current Direction	nFET	nACK	Mode
< OVP Threshold	< V_{IN}	V_{IN} à V_{OUT}	On	Low	Charge
< OVP Threshold	> V_{IN}	V_{OUT} à V_{IN}	On	Low	OTG
≥ OVP Threshold	< V_{IN}	No Current flowing	Off	Hi-z	OVP
≥ OVP Threshold	> V_{IN}	V_{OUT} à V_{IN} (via the junction body diode)	Off	Hi-z	OVP
< UVLO Threshold	< V_{IN}	No Current flowing	Off	Hi-z	UVLO
Don't Care	Don't Care	No Current flowing	Off	Hi-z	Thermal Shutdown

PCB Layout Consideration

1. All the peripherals should be placed as close to the device as possible. Place the input capacitor C_{IN} on the top layer and close to V_{IN} pin, and place the output capacitor C_{OUT} on the top layer and close to V_{OUT} pin.

2. Exposed Pad (EP) connects to V_{IN}, which is USB connector, and conducts large current during normal operation as well as surge protection. Route it out as straight, wide and short as possible. Also keep other traces away from it to minimize possible EMI coupling.

3. GND pin 2 & 3 conducts large current during surge protection. Make sure no signal trace blocks the path for current flow.

4. Use rounded corners on the power trace to decrease EMI.

5. If R_1 and R_2 are used, route OVLO line as short as possible to reduce parasitic capacitance.

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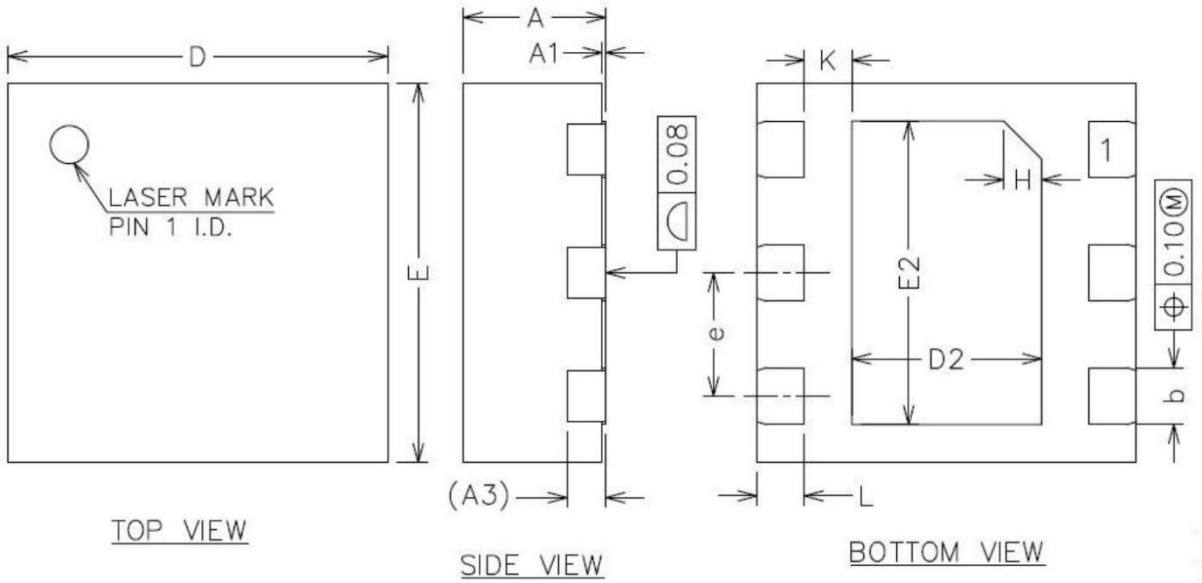
Package Outline Drawing



SIDE VIEW

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.527	0.550	0.577
A1	0.00	0.02	0.05
A3		0.20REF	
b	0.25	0.30	0.35
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.90	1.00	1.10
E2	1.50	1.60	1.70
e	0.55	0.65	0.75
K	0.15	0.25	0.35
L	0.20	0.25	0.30
H		0.20REF	