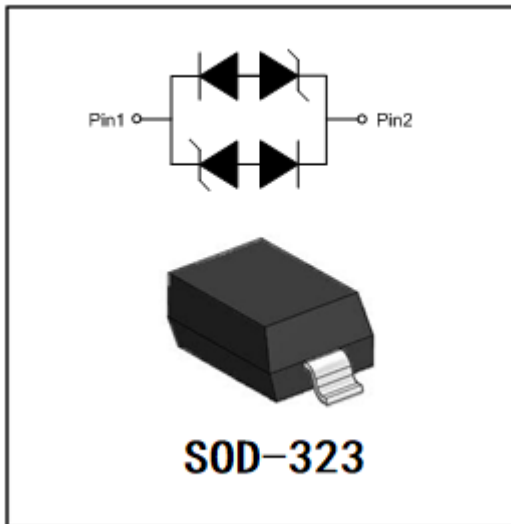


1-Line Low Capacitance Bi-directional TVS Diode



Features

- 340W peak pulse power (8/20 μ s)
- Ultra low capacitance: 1pF typical
- Ultra low leakage: nA level
- Operating voltage: 3.3V
- Low clamping voltage
- Protects one power line or data line
- Complies with following standards:
 - IEC 61000-4-2 (ESD) immunity test
 - Air discharge: \pm 30Kv
 - Contact discharge: \pm 30kV
 - IEC61000-4-5 (Lightning) 30A (8/20 μ s)
- RoHS Compliant

Marking Information



■ Maximum Ratings

PARAMETER	SYMBOL	VALUE	UNIT
Peak Pulse Power (8/20 μ s)	Ppk	340	W
Peak Pulse Current (8/20 μ s)	I _{PP}	21	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V _{ESD}	\pm 30 \pm 30	KV
Operating Temperature Range	T _J	-55 to +125	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C

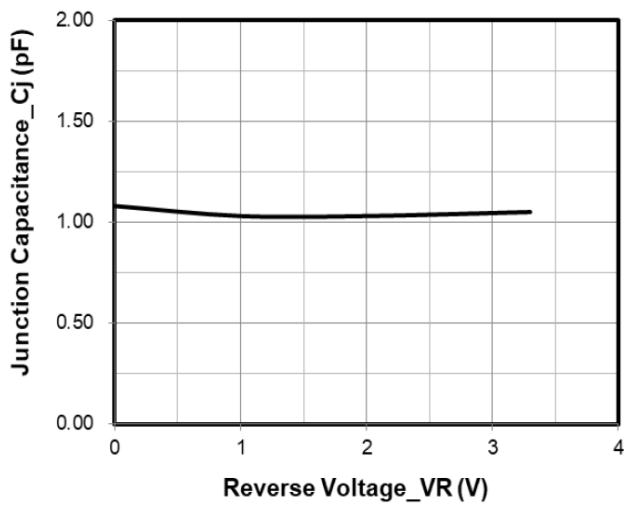


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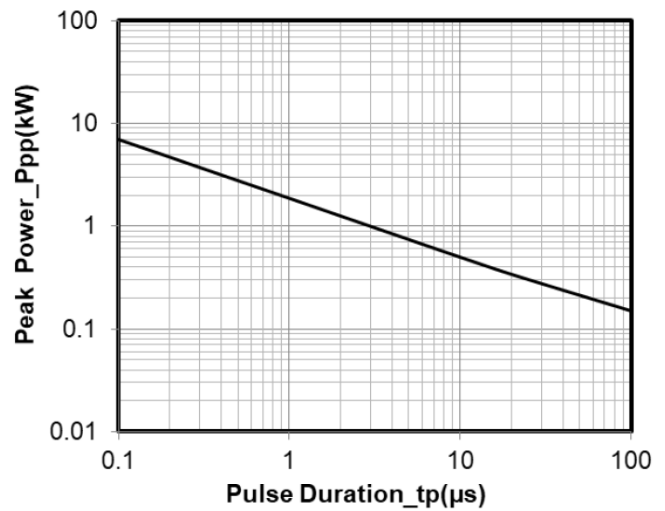
■ Electrical Characteristics (T_a=25°C Unless otherwise specified)

PARAMETER	SYMBOL	UNIT	CONDITIONS	MIN	TYP	MAX
Reverse Working Voltage	V _{RWM}	V				3.3
Reverse breakdown voltage	V _{BR}	V	I _{BR} = 2μA	3.5		
Reverse Leakage Current	I _R	μA	V _{RWM} = 3.3V			0.2
Clamping Voltage	V _C	V	I _{PP} = 1A (8/20μs pulse)			7
Clamping Voltage	V _C	V	I _{PP} = 21A (8/20μs pulse)			16
Junction Capacitance	C _J	pF	V _R = 0V, f = 1MHz		1	

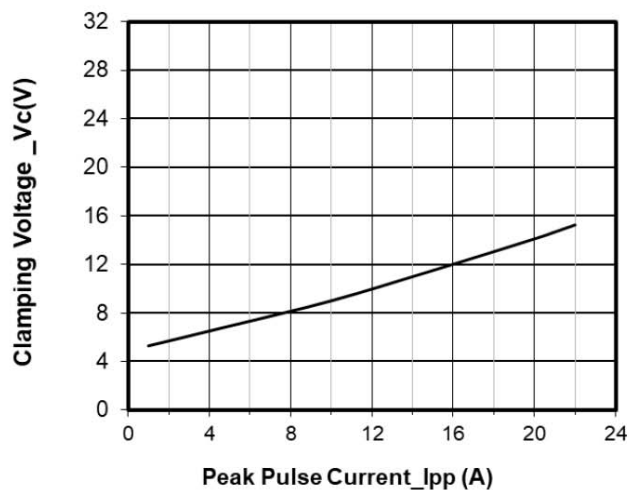
■ Characteristics (Typical)



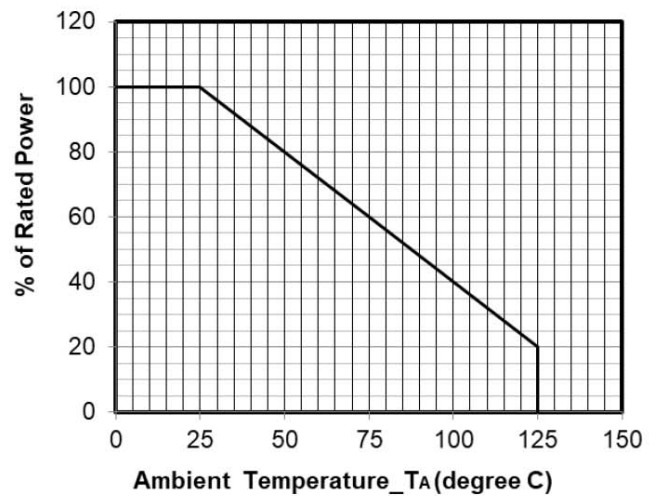
Junction Capacitance vs. Reverse Voltage



Peak Pulse Power vs. Pulse Time



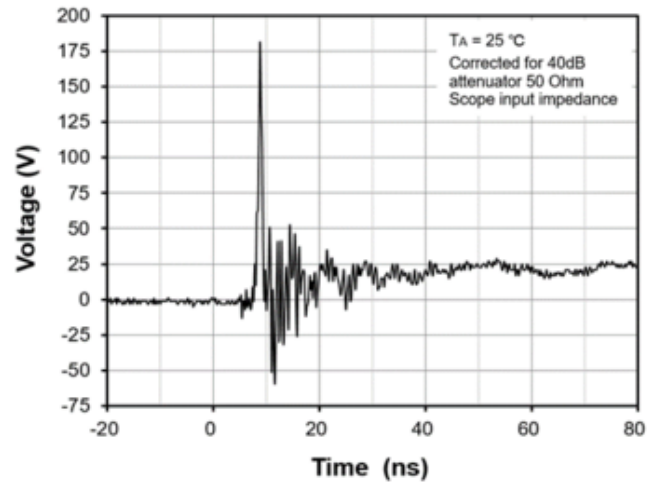
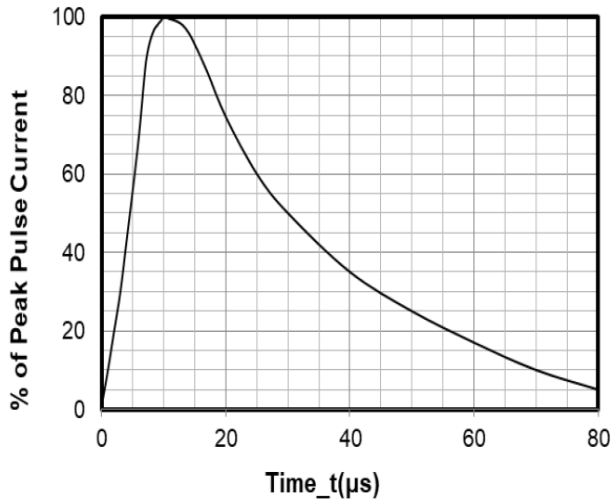
Clamping Voltage vs. Peak Pulse Current



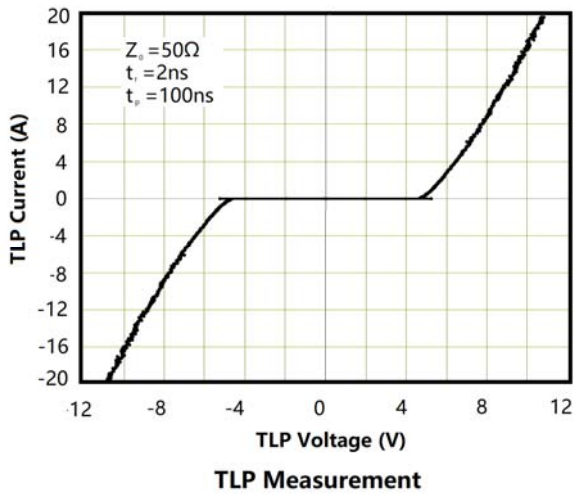
Power Derating Curve



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8 X 20μs Pulse Waveform

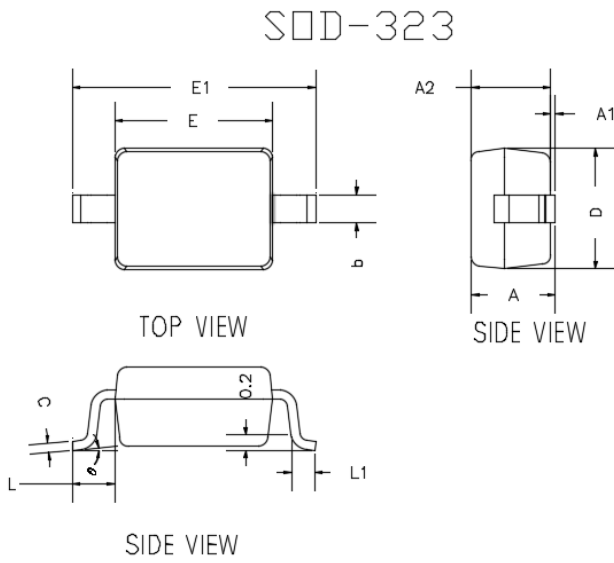


TLP Measurement



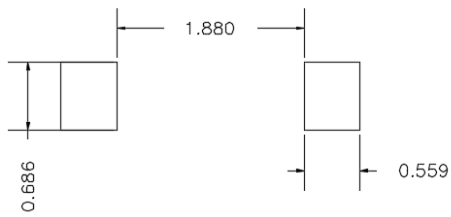
ESDSL3V3D3BA

■ Outline Dimensions



DIMENSIONS				
DIM	INCHES		MM	
	MIN	MAX	MIN	MAX
A	---	0.0393	---	1.0000
A1	0.0000	0.0039	0.0000	0.1000
A2	0.0314	0.0354	0.8000	0.9000
b	0.0098	0.0157	0.2500	0.4000
c	0.0031	0.0059	0.0800	0.1500
D	0.0472	0.0551	1.2000	1.4000
E	0.0629	0.0709	1.6000	1.8000
E1	0.0984	0.1063	2.5000	2.7000
L	0.0187TYP		0.475TYP	
L1	0.0098	0.0157	0.250	0.400
θ	0°	8°	0°	8°

■ Soldering Footprint



UNIT : mm

SUGGESTED SOLDER PAD LAYOUT



ESDSL3V3D3BA

Disclaimer

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